What is claimed is:

1. An apparatus capable of making optimal differential and single-ended measurement interfaces, comprising:

a first summation element operable to receive a first input to be measured and a first final offset voltage input, wherein a first summation element output is the algebraic sum of the first input and the first final offset voltage input;

a second summation element operable to receive a second input to be measured and a second final offset voltage input, wherein a second summation element output is the algebraic sum of the second input and the second final offset voltage input;

a first switch operable to receive a first offset voltage and to enable and disable the first final offset voltage;

a second switch operable to receive a second offset voltage and to enable and disable the second final offset;

a differential amplifier operable to receive first and second summation element outputs as differential inputs, having a differential amplifier output which is determined by the difference between the differential inputs;

a third summation element operable to receive the differential amplifier output signal and a third final offset voltage as inputs, and produce a third summation element output which is the algebraic sum of the differential amplifier output signal and the third final offset voltage; and

a third switch operable to receive a third offset voltage and to enable and disable the third final offset voltage.

2. The apparatus of claim 1 wherein the first switch is controllable manually, or digitally locally, or digitally external to the apparatus.

3. The apparatus of claim 1 wherein the second switch is controllable manually, or digitally locally, or digitally external to the apparatus.

4. The apparatus of claim 1 wherein the third switch is controllable manually, or digitally locally, or digitally external to the apparatus.

5. The apparatus of claim 1 wherein the first offset voltage is derived using analog or digital techniques.

6. The apparatus of claim 1 wherein the second offset voltage is derived using analog or digital techniques.

7. The apparatus of claim 1 wherein the third offset voltage is derived using analog or digital techniques.

8. The apparatus of claim 1 wherein the first summation element output comprises a voltage or a current.

9. The apparatus of claim 1 wherein the second summation element output comprises a voltage or a current.

10. The apparatus of claim 1 wherein the third summation element output comprises a voltage or a current.

11. The apparatus of claim 1 wherein one or more of the first summation element, the second summation element, the third summation element, the first switch, the second switch, the third switch, and/or the differential amplifier are implemented using analog techniques or software techniques.

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12. The apparatus of claim 1 wherein the apparatus is mounted in a probe.

13. A system capable of making optimal differential and single-ended measurement interfaces, comprising:

a first summation element operable to receive a first input to be measured and a first final offset voltage input, wherein a first summation element output is the algebraic sum of the first input and the first final offset voltage input;

a second summation element operable to receive a second input to be measured and a second final offset voltage input, wherein a second summation element output is the algebraic sum of the second input and the second final offset voltage input;

a first switch operable to receive a first offset voltage and to enable and disable the first final offset voltage;

a second switch operable to receive a second offset voltage and to enable and disable the second final offset;

a differential amplifier operable to receive first and second summation element outputs as differential inputs, having a differential amplifier output which is determined by the difference between the differential inputs;

a third summation element operable to receive the differential amplifier output signal and a third final offset voltage as inputs, and produce a third summation element output which is the algebraic sum of the differential amplifier output signal and the third final offset voltage;

a third switch operable to receive an offset voltage and to enable and disable a third final offset voltage; and

control of the first switch, the second switch, the third switch, the first offset, the second offset, or the third offset which is applied from a source or sources external to the apparatus.

14. The apparatus of claim 13 wherein said control is generated by sources within the probe.

15. The apparatus of claim 13 wherein said control is generated by sources external to the probe.

16. A method of optimizing single-ended and differential inputs received by the measurement interface, comprising:

selectively modifying offset from a first input;

selectively modifying offset from a second input;

generating the algebraic difference of the first and second inputs after offset has been selectively modified from said first and second inputs; and

adjusting a final output offset to nullify a differential amplifier offset or to establish a desired DC output component on an output of the measurement interface.

17. The method of claim 16, further comprising:

enabling a first switch to allow variability of a first final offset;

disabling a second switch to force a zero value for a second final offset;

disabling a third switch to force a third final offset to zero; and

adjusting a first offset voltage to produce zero static DC level of the output.

18. The method of claim 16, further comprising:

enabling a first switch to allow variability of a first final offset;

disabling a second switch to force zero for a second final offset;

enabling a third switch to allow variability of a third final offset;

adjusting a first offset voltage for zero offset at a first differential amplifier input; and

adjusting a third offset voltage to null the differential amplifier offset or to establish an output DC offset of the output.

19. The method of claim 16, further comprising:

enabling a first switch to allow variability of a first final offset;

enabling a second switch to allow variability of a second final offset;

disabling a third switch to force a third final offset to zero;

adjusting a first offset voltage for zero offset at a first differential amplifier input; and

adjusting a second offset voltage for zero offset at a second differential amplifier input.

20. The method of claim 16, further comprising:

enabling a first switch to allow variability of a first final offset;

enabling a second switch to allow variability of a second final offset;

enabling a third switch to allow variability of a third final offset;

adjusting a first offset voltage for zero offset of a first differential amplifier input;

adjusting a second offset voltage for zero offset of a second differential amplifier input; and

adjusting a third offset voltage to null the differential amplifier offset or to establish an output DC offset of the output.

21. The method of claim 16, further comprising:

disabling a first switch to force a first final offset to zero;

enabling a second switch to allow variability of a second final offset;

enabling a third switch to allow variability of a third final offset;

adjusting a second offset voltage for zero offset at a differential amplifier input; and

adjusting a third offset voltage to null a differential amplifier offset or to establish an output DC offset of the output.

22. The method of claim 16, further comprising:

disabling a first switch to force a first final offset to zero;

disabling a second switch to force a second final offset to zero;

enabling a third switch to allow variability of a third final offset; and

adjusting a third offset voltage to null the differential amplifier offset or to establish an output DC offset of the output.

23. The method of claim 16, further comprising:
disabling a first switch to force a first final offset to zero;
disabling a second switch to force a second final offset to zero; and
disabling a third switch to force a third final offset to zero; and
performing measurements without signal offset modifications by the measurement interface.

24. The method of claim 16, further comprising:
disabling a first switch to force a first final offset to zero;
enabling a second switch to allow variability of a second final offset;
disabling a third switch to force a third final offset to zero; and
adjusting a second offset voltage for zero offset of a differential amplifier input.

25. An apparatus operable to receive and operate on first and second inputs of a measurement interface, comprising:

first means for selectively modifying offset from the first input;

second means for selectively modifying offset from the second input;

means for generating the algebraic difference of first and second inputs after offset has been selectively removed from each; and

third means for selectively modifying a final output offset of an output.

26. A measurement interface capable of optimizing single-ended and differential inputs received by the measurement interface, comprising:

a first summation element operable to selectively modify offset from a first input and generate a first summation element output;

a second summation element operable to selectively modify offset from a second input and generate a second summation element output; and

a difference element that receives the first and second summation element outputs and generates the difference between said first and second summation element outputs at an output of the difference element.

27. The interface of claim 26, wherein the difference element is a differential amplifier.

28. The interface of claim 26, further comprising:

a third summation element operable to selectively modify offset from the output.